REMARKS/ARGUMENTS

Claims 1-8 remain pending in this application. No claim amendments have been made. No new matter has been added.

Withdrawn Claims

Applicant has canceled the non-elected claims without prejudice or disclaimer.

Claim Rejections under 35 U.S.C. §103

Claims 1 and 6-8 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Katz, U.S. Patent No. 3,521,242 and Yamada, U.S. Patent No. 5,986,924; and claims 2-5 are rejected under 35 U.S.C. §103(a) as being unpatentable over Katz and Yamada, as applied to claim 1 and further in view of Kotani, U.S. Patent No. 6,638,799. Applicants request reconsideration of the rejections for the following reasons.

The present invention is directed to providing a semiconductor device mounted with a SRAM memory using an SOI substrate which ensures stable operation while maintaining space requirements. SRAMs mounted on a processor are required to operate at low voltages in which the operation margin for the write/read operation is reduced, which has a great effect on device operation, thereby making it difficult for a SRAM cell to operate stably. Further, the threshold voltage is hard to reduce because leakage current may increase, causing the operation speed to drop at a low speed (see page 6, lines 4-11).

For SRAM memory cells, the regions forming the channels of the drive MISFETs are in a floating state, while the regions forming the channel of the transfer MISFETs are controlled,

especially by using Dynamic-Threshold-Voltage Metal Oxide Semiconductor Field Effect Transistor (DTMOSFET). As shown in FIG. 4, it is useful to couple the gate electrodes of the N-channel type DTMISFETs (DTMN1,DTMN2) to the channel regions, respectively. The MISFET, of which the gate and channel region is coupled, has such a characteristic that it is capable of varying its threshold voltage dynamically, enabling the potential responsive to the voltage applied to the word line WL to be supplied to the channel formation regions of the N-channel type DTMISFETs (DTMN1,DTMN2). When not being selected, the N-channel type DTMISFETs (DTMN1,DTMN2)connected to the word line are always on an off state, wherein a low potential (ground potential) is supplied to the channels and the channel region is not on a floating state, reducing leakage current. On the other hand, when being selected, the potentials of the channels go "H" and their threshold voltages drops, thereby the memory cell current increases, enabling high-speed operation. See, page 14, line 9 -page 15, line 11 of the specification.

Katz, on the other hand, discloses a typical SRAM circuit, but does not disclose or teach the claimed combination of independent claims 1 and 6. Yamada discloses a SRAM circuit wherein both channel regions of the transfer and driver MOSs (21 and 23) are commonly coupled to the word line (WL0)(see Figure 1), in order to provide a SRAM wherein high-speed and low-voltage operation can be achieved with the disclosed circuit configuration (*see*, col. 3, lines 47-50 of Yamada). However, Yamada does not disclose or teach that which is lacking I Katz, with respect to the claimed invention.

In the present invention, since each of the channel regions of the driver MISFETs is in a state of floating. However, in Yamada, one having ordinary skill in the art would conclude that

the coupling between the channel region of the transfer MOS 21 and the word line WL0 causes the spatial overhead to increase while the coupling between the channel region of the driver MOS 23 and the word line WL0 can be made small. Therefore, the circuit disclosed in Yamada cannot achieve the object of ensuring stable operation of the circuit while maintaining sufficiently decreased space requirements, as in the present invention. Accordingly, the present invention as claimed in claims 1 and 6-8 is not obvious over the combination of Katz and Yamada under 35 U.S.C. § 103(a) and therefore the rejection should be withdrawn.

Kotani is relied upon for disclosing a memory device being on a chip with first and second semiconductor layers separated by an insulating layer. However, the reference does not make up[for the deficiencies in the Katz and Yamada combination, which is applied to independent claim 1, from which claims 2-5 depend. Accordingly, the 35 U.S.C. § 103(a) rejection of claims 2-5 should be withdrawn.

CONCLUSION

In view of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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